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CERTIFICATION

I, the below named translator, hereby declare that: my name and post office address are as stated below; that I am knowledgeable in the English and German languages, and that I believe that the attached text is a true and complete translation of the German priority document bearing No. 102 44 664.4, filed with the German Patent Office on September 24, 2002.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Description

Electronic component with semiconductor chips in a stack, and a method for producing it

The invention relates to an electronic component with semiconductor chips in a stack and to a method for producing this component. In particular, the invention relates to an electronic component with a stack formed from a logic chip based on flipchip technology and a memory module whose operation has been tested and which uses bonding technology.

The aim of achieving ever greater circuit densities is leading to greater system integration, with increasing attempts being made to arrange two or more semiconductor chips in a stack. In this case, a complete component frequently has to be rejected merely because the memory chip is not operating, even though the logic chip is intrinsically serviceable.

The object of the invention is to specify a method by means of which electronic components with semiconductor chips in a stack can be produced at low cost, and with the electronic components having reduced failure rates in the functional tests.

The object is achieved by the subject matter of the independent claims. Advantageous developments of the invention are described in the dependent claims.

According to the invention, a method is provided for producing an electronic component with semiconductor chips in a stack.

First of all, an interposer is produced for this purpose, having connecting pads for flipchip connections in a central area. Furthermore, the interposer has connecting pads for bonding connections in its edge areas. The interposer is thus able to electrically connect both semiconductor chips using flipchip technology and semiconductor chips using bonding technology in a stack to external contacts of the electronic component. Next, a first electronics module which is in the form of a semiconductor chip and uses flipchip technology is fitted to this interposer, which has connecting pads for flipchip connections in its central area.

In parallel with this, at least one second electronics module is produced which, in addition to its semiconductor chip, has an interposer structure with external contact surfaces. This second electronics module is fitted as an upper module to the first electronics module, such that the passive rear faces of the first and of the second electronics modules rest one on top of the other. Bonding connections are then produced between the external contact surfaces of the second upper electronics module and the connecting pads in the edge areas of the interposer. Finally, the stacked electronics modules are then packed to form an electronic component with a plastic packaging compound being fitted to the interposer.

This method has the advantage that the fitting of the interposer structure to the active upper face of the semiconductor chip of the upper electronics module creates an intermediate substrate, which provides the upper electronics module with the necessary robustness for handling in a test procedure. In addition, external contacts can be fitted at least temporally to the external contact surfaces of the interposer structure, in order to test the operation of the

upper electronics module independently of the stack in extreme temperature cycles. These external contacts, which may be required for test connectors that are specified, can be removed again before the upper electronics module is installed in the stack, in order to provide the external contact surfaces for bonding during assembly of the electronic component.

The increased robustness of the upper electronics module allows the bonding connections between the external contacts at the edge of the interposer structure of the upper electronics module and the connecting pads for bonding connections in the edge areas of the interposer to be produced without any problems and with increased reliability once the passive rear faces of the electronics module have been brought together. This is because the brittle material of the semiconductor chip for the upper module is relieved of loads during the bonding process by the intermediate mount for the interposer structure, so that the risk of microscopic cracks being formed in the semiconductor chip during the bonding process is reduced. In order to provide a bonding connection, the normals to the surface of the connecting pads for bonding connections and the normals to the surface of the external contact surfaces of the upper electronics module point in the same direction.

A further possible advantage of the method is that it is also possible to use components with a larger passive rear face than the semiconductor chips arranged underneath them as the upper electronics modules to be bonded, because the robustness of the upper electronics modules is increased by the interposer structure with an intermediate substrate in the area of the external contact surfaces to be bonded, and the

bonding process does not take place on the semiconductor chip, but on the intermediate substrate. This is particularly advantageous when a logic chip is used as the first lower electronics module, and a memory chip with a larger area is used as the second upper electronics module.

Before the upper electronics module is fitted to the passive rear face of the semiconductor chip of the lower electronics module, the upper electronics module can thus be subjected to temperatures of -50°C to 150°C, during which its serviceability is tested. In the process, the module is operated electrically. To do this, the interposer structure, with its external contact surfaces, can be matched to the grid size of appropriate test connectors. The temporary fitting of external contacts to the external contact surfaces of the interposer structure as mentioned above can also provide improved contact with the test connectors. After removal of the temporary fitted external contacts, the external contact surfaces are available for fitting bonding connections during the assembly of the electronic component.

According to the invention, all the signal connections on the upper electronics module can be accessed during a functional test. This accordingly allows a more valid test result, not least because access to all the signal connections of the upper electronics module independently of the other electronics modules in the stack is no longer possible after assembly of the electronic component. If a functional test such as this for the upper electronics module is carried out before the assembly of the electronic component, then the overall yield is improved, and this results in considerable cost advantages. This is because at least one or both of the electronics modules is or are tested in advance, thus making

it possible to ensure that even electronics modules with a potentially high failure probability, such as memory chips, are used only after they have been tested in detail as described above. The stacking of electronics modules one above the other also saves space, increases the circuit density, and the costs are optimized. Furthermore, the electrical characteristics are improved, since this results in short bonding connections, and this is associated with the reduction in parasitic inductances.

The passive rear faces of the electronics modules can advantageously be adhesively bonded to one another. Conductive adhesives can be used for this purpose, for example when the rear faces of the electronics modules are at the same potential. If there are intended to be potential differences between the rear faces of the electronics modules, then insulating adhesives can be used.

The bonding connections between the external contacts on the upper electronics module and the connecting pads in the edge area of the interposer can be produced by means of thermocompression bonding. In the process, a bonding head is formed on one of the surfaces to be connected, and the bonding wire is initially connected from this bonding head in the direction of the normal to the surface before it can be bent toward the second surface, where it is electrically bonded to the second surface, forming a bonding clip. While the bonding clip can be fitted to the second surface virtually tangentially with respect to that surface, the bonding head with the curved bonding wire must be at a minimum height above the bonded surface. It is therefore advantageous for the bonding head first of all to be produced on the connecting pad for the bonding connections in the edge area of the

interposer, with the bonding clip not being formed on the external contact surface of the interposer structure of the upper electronics module until this has been done. This also minimizes the component height of the electronic component with semiconductor chips in a stack.

A central bonding channel can be incorporated in the interposer structure of the upper electronics module. The central bonding connections of this central bonding channel are electrically conductively connected to the external contact surfaces via bonding fingers and via interposer lines. The external contact surfaces may be distributed over edge areas of the upper electronics module, thus simplifying the process of bonding to the connecting pads in the edge areas of the wiring substrate, and allowing short bonding wire lengths.

The central bonding connections in the bonding channel have smaller dimensions than the bonding connections on the external contact surfaces, so that they are to this extent sufficiently protected just by the bonding channel that the upper electronics module can be subjected to a functional test of careful handling with an open unprotected bonding channel. However, the bonding channel may advantageously be covered by a plastic protective sheath, with the central bonding connections in the bonding channel being embedded, before the upper electronics module is subjected to a functional test. This has the advantage that it simplifies the handling both during the functional test and during the subsequent assembly process, and reliably prevents damage to the central bonding connections.

A printed circuit board which is metallized on both sides may be used as the interposer, whose metal plating is structured

on its upper face and on its lower face. The structure on the upper face may have contact connecting pads for flipchip connections in a central area. Connecting pads for bonding connections may be provided in the edge areas of the upper face. The structured metal plating on the lower face of the printed circuit board may have external contact surfaces, which can be electrically connected to the connecting pads via through-contacts and via interposer lines. An interposer such as this based on a printed circuit board which is metallized and structured on both sides can be produced at low cost, and has a considerable price advantage over interposers based on ceramic.

Once the electronics modules to be formed into a stack have been fitted to an interposer that has been prepared in this way, the electronics modules can be embedded in a filled epoxy resin by means of a transfer molding process. This packing process can be carried out simultaneously for two or more electronic components, provided that the interposer that is used has an appropriate number of component positions in which electronics modules are stacked and bonded. While the bonding connections are severely loaded during the transfer molding process, owing to the high pressure and the flowing characteristics of the filled epoxy resin, packing of the electronics modules in a plastic package by means of a dispensing process provides considerably better protection.

Finally, external contacts can be fitted to the external contact surfaces of the interposer. These external contacts may have solder balls, with a solder resist varnish layer surrounding the external contact surfaces preventing the material of the external contacts from wetting interposer lines, for example.

The invention also relates to an electronic component with semiconductor chips in a stack and which has an interposer. Connecting pads for flipchip connections are provided in a central area of the interposer. The interposer has connecting pads for bonding connections in its edge areas. Contact areas on a first lower electronics module, which is in the form of a semiconductor chip, are connected to the connecting pads in the central area of the interposer. A second upper electronics module has a semiconductor chip with an interposer structure, and with external contact surfaces. The upper electronics modules are arranged on the lower electronics modules such that the passive rear faces of the electronics modules rest one on top of the other. In order to electrically connect the upper electronics module to the interposer, bonding connections are provided between the external surfaces of the upper electronics module and the connecting pads in the edge areas of the interposer.

The stack formed from at least one semiconductor chip using flipchip technology and from an electronics module with an interposer structure and with external contact surfaces is surrounded by a component package. An electronic component formed from a combination of the semiconductor chip as the first lower electronics module and from a second upper electronics module, which is largely packaged, has the advantage that the external contact surfaces on the upper electronics module can be used in order to test the serviceability of the largely packaged upper electronics module in extreme temperature conditions before assembly to form an electronic component, so that a reliable statement can be made on whether the stack has at least one fully serviceable upper electronics module. The stacking process reduces the amount of space required, and increases the

circuit density. The capability to carry out functional tests on the upper electronics module separately allows cost optimization and a capability to reliably predict the final electrical characteristics of the electronic component.

These advantages are particularly important when the lower electronics module is a logic chip and the upper electronics module is a memory chip with an interposer structure and with external contact surfaces. Memory chips such as these have a relatively high failure rate during functional testing in extreme temperatures between -50°C and 150°C. This failure rate can be reduced for the electronic component with a stack comprising a logic chip and a memory chip, if the memory chip is provided in advance with an interposer structure with external contact surfaces, thus allowing independent complete functional testing before the rest of the stack is formed.

A further advantage is that the external contact surfaces on the upper electronics module can be placed in the edge areas of the upper electronics module, owing to the wiring structure, thus allowing extremely short bonding connections from the external contact surfaces to the connecting pads in the edge areas of the interposer. The short bonding connections result in adequate bonding wire robustness, so that a highly filled epoxy resin can be used as the material for the plastic package, without having to take any particular precautions for protection of the bonding connections.

The interposer structure with its intermediate substrate and the external contact surfaces on the upper electronics module at the same time improves the mechanical robustness of this electronics module, thus improving the overall reliability of the electronic component, and in the process reducing the risk

of microscopic cracks being formed in the semiconductor chip during the bonding process, since the bonding process is not carried out directly on the semiconductor chip.

The interposer has a printed circuit board which is metallized and structured on both sides. This printed circuit board has through-contacts as an electrical connection between the structured metal layers on the upper face and on the lower face of the printed circuit board. The lower face of the printed circuit board has external contact surfaces for external contacts. In its central area, the upper face of the printed circuit board has the connecting pads for the flipchip connections and, in its edge areas, it has the connecting pads for bonding connections. The external contact surfaces on the lower face of the printed circuit board are electrically connected via through-contacts and via interposer lines to the connecting pads on the upper face. An interposer such as this based on a printed circuit board can be produced at low cost in comparison to interposer films or interposers based on ceramics.

An adhesive layer is arranged between the passive rear faces of the electronics module, which rest one on top of the other. If the adhesive layer is formed by a conductive adhesive, the rear faces of the electronics module may be at the same potential. An adhesive layer composed of an insulating adhesive may then, for example, be provided between the two rear faces of the electronics modules, if a potential difference is desired on the rear faces between the two electronics modules.

The upper electronics module has a central bonding channel with central bonding connections on its active upper face.

These central bonding connections are connected to the external contact surfaces via the interposer structure that is arranged on the active upper face. This bonding channel may have a protective sheath for its central bonding connections, thus forming a material boundary between a protective sheath such as this and the plastic package for the electronic component. A bonding channel such as this with central bonding connections is used in particular for memory chips, in order to make use of the relatively large upper active face of the memory chips on both sides of the bonding channel for the arrangement of external contact surfaces.

The bonding connections between the external contact surfaces and the connecting pads in the outer areas of the interposer may use a bonding wire which is subdivided into a bonding head and a bonding clip. The bonding head may be arranged on one of the connecting pads of the interposer, while the bonding clip is arranged on the corresponding external contact surface of the upper electronics module. This configuration of the bonding connections has the advantage that the bonding clip occupies a smaller height than the bonding head, so that the overall height of the electronic component can be minimized.

The invention also provides for an intermediate space to be formed for the contact areas between the active upper face of the semiconductor chip in the lower electronics module and the upper face of the interposer. This intermediate space is filled with an underfilling material, which includes a highly filled plastic with a filling level of 80 to 95% by weight. This high filling level of the underfilling material allows the thermal expansion behavior of the underfilling material to be largely matched to the thermal expansion behavior of the semiconductor chip.

In summary, it can be stated that a memory chip in a BOC package (board on chip package), for example, can be used as a second upper module in an electronic component, before its chip rear face, which remains free, is adhesively bonded to a logic chip using flipchip technology, can be burned into its package at this stage, and can be subjected and tested in extreme temperatures. Optimization of the bonding process during connection of the upper memory chip to the interposer also allows a memory chip to be stacked in a space-saving manner on a logic chip.

The interposer structure that is fitted to the memory chip together with its intermediate substrate result in a highly flexible packaging concept in terms of design and routing, as well as interposer routing. This package for the upper memory chip makes matching easier when using memory modules from different suppliers or when technology changes occur, since the interposer allows matching to take place without having to make any changes to the interposer with the lower flipchip module. This results in a lower-cost, flexible structure, with a matching capability for forming a stack comprising an electronics module using flipchip technology and an electronics module using bonding technology.

The invention will now be explained in more detail with reference to the attached figures, in which:

Fig. 1 shows a schematic cross section through a first embodiment of an electronic component according to the invention,

Fig. 2 shows a schematic cross section through a second embodiment of an electronic component according to the invention,

Fig. 3 shows a schematic cross section through a third embodiment of an electronic component according to the invention,

Fig. 4 shows a schematic cross section through a fourth embodiment of an electronic component according to the invention,

Figs. 5 to 11 show schematic cross sections through intermediate products during the production of the first embodiment of the electronic component according to the invention,

Fig. 5 shows a schematic cross section through an interposer,

Fig. 6 shows a schematic cross section through an interposer, with a first electronics module fitted to it,

Fig. 7 shows a schematic cross section through a second electronics module with an unprotected bonding channel,

Fig. 8 shows a schematic cross section through the second electronics module as shown in Fig. 7, with a protected bonding channel,

Fig. 9 shows a schematic cross section through a stack formed by the first electronics module and the second electronics module on the interposer shown in Fig. 5,

Fig. 10 shows a schematic cross section through a stack as shown in Fig. 9, after the fitting of bonding connections,

Fig. 11 shows a schematic cross section through an electronic component after the stack as shown in Fig. 10 has been packed in a component package,

Fig. 12 shows a schematic cross section through an electronic component after the fitting of external contacts to the interposer for the electronic component.

Fig. 1 shows a schematic cross section through a first embodiment of an electronic component 1 according to the invention. The base of this electronic component 1 forms an interposer 5 with an upper face 36 and with a lower face 40, which at the same time forms the lower face of the electronic component 1. External contacts 30 in the form of contact balls are arranged on the lower face 40 and are soldered to external contact surfaces 27 on the interposer 5. These external contact surfaces 27 on the interposer 5 are connected via through-contacts 26 and via interposer lines 25 for the interposer 5 to connecting pads 6 and 60 on the upper face 36 of the interposer 5. In this first embodiment of the invention, the interposer 5 has a printed circuit board 23 as the mount material.

Connecting pads 6 for connection to flipchip contacts are arranged in a central area 7 on the upper face 36 of the interposer 5. Connecting pads 60 for bonding connections are arranged in the edge areas 10 on the upper face 36 of the interposer 5. At least one logic chip 28 with its contact areas 24 is fitted to the connecting surfaces 6 in the central area 7, via flipchip connections 8, as a first lower

electronics module 9. An adhesive bonding layer 31 is arranged on the passive rear face 15 of this first electronics module 9 and is used for arranging a second upper electronics module 12 on the first lower electronics module 9.

The second electronics module 12 is a memory chip 39, which has a central bonding channel 19 on its active upper face 32, with central bonding connections 111. These central bonding connections 111 for the bonding channel 19 are connected via bonding fingers 20 in the interposer structure 13 to external contact surfaces 14 on the upper electronics module 12. The interposer structure 13 has an intermediate substrate 41, on whose edge areas the external contact surfaces 14 are arranged. The external contact surfaces 14 are connected via bonding heads 33 from bonding wires 18 to the connecting pads 60 in the edge area 10 of the interposer 5, forming a bonding clip 34.

A component package 29 surrounds this stack 4 that is formed from at least one lower logic chip 28 and one upper memory chip 39, as well as the bonding connections 18 between the upper memory chip 39 and the interposer 5. An underfilling material 37, which is in the form of highly filled plastic with a filling level of between 80 and 95% by weight, fills an intermediate space between the active upper face 35 of the logic chip 28 and the upper face 36 of the interposer 5, and embeds the contact areas 24 of the logic chip 28. The high filling level ensures that the thermal expansion behavior of the underfilling material 37 is largely matched to the thermal expansion behavior of the semiconductor material of the logic chip 28. A protective sheath 22 covers the bonding channel 19, and protects the central bonding connection 111 for the memory chip 39. A material boundary 38 is formed between the

protective sheath 22 and the surrounding plastic packaging compound 17 of the component package 29.

This electronic component 1 thus has a stack 4 comprising a semiconductor chip 2 using flipchip technology and a virtually completely packaged electronics module 12. The serviceability of this electronics module 12 will have been tested in extreme temperatures between -50 and 150°C before it is installed in the electronic component 1. This serviceability test can be carried out either by connecting the external contact surfaces 14 of the upper electronics module 12 to an appropriate test connector, or by external contacts being temporarily fitted to the external contact surfaces 14, with these being removed again after the test and before installation in the electronic component 1.

In one exemplary embodiment, which is not shown here, the underfilling material 37 is omitted, with the gap between the active upper face 35 and the upper face 36 being filled with the plastic packaging compound 17.

Fig. 2 shows a schematic cross section through a second embodiment of the electronic component 1 according to the invention. Components with the same functions as those in Fig. 1 are identified by the same reference symbols, and will not be explained once again.

One difference between the electronic component 1 shown in Fig. 1 and the second embodiment of the electronic component 1 according to the invention is that the bonding wires 18 for the bonding connections 11 are arranged with bonding heads 33, which occupy their component height, on the connecting pads 60 in the edge areas 10 of the interposer 5. The relatively flat

bonding clip 34 for a bonding connection 11 such as this is arranged on the external contacts 14 of the upper electronics module 12. This makes it possible to limit the component height of the electronic component 1 by the protective sheath 22 for the bonding channel 19. The electronic component 1 is thus not as high as the electronic component 1 shown in Fig. 1. The material boundary 38 between the plastic packaging compound 17 and the plastic of the protective sheath 22 for the bonding channel 19 is thus restricted to the edge faces of the protective sheath 22.

Fig. 3 shows a schematic cross section through a third embodiment of an electronic component 1 according to the invention. Components with the same functions as those in the previous figures are identified by the same reference symbols, and will not be explained again.

The configuration of the stack formed by the electronics modules 9 and 12 in the third embodiment of the invention is the same as in the first embodiment of the invention as shown in Fig. 1. However, in this case, the bonding channel 19 for the upper electronics module 12 is covered by the plastic packaging compound 17, so that no material boundary 38 as shown in Fig. 1 is formed. During assembly of this electronic component 1, the method step of embedding the central bonding connections 111 for the bonding channel 19 in a protective sheath 22 is avoided. Nevertheless, the upper electronics module 12 can be tested for serviceability before being installed in an electronic component 1 such as this, and has the external contact surfaces 14 required for the functional test.

Fig. 4 shows a schematic cross section through a fourth exemplary embodiment of an electronic component 1 according to the invention. Components with the same functions as those in the previous figures are identified by the same reference symbols, and will not be explained again.

The internal configuration of the electronic component 1 in the fourth embodiment of the invention corresponds to the configuration of the electronic component 1 shown in Fig. 2. However, the protective sheath 22 for the bonding channel 19 for the upper electronics module 12, has been omitted in order to save costs. The electronic component 1 is thus produced at low cost, with a minimal component height.

Figs. 5 to 12 show schematic cross sections through intermediate products during the production of the first embodiment of an electronic component 1 according to the invention. Components with the same functions as those in the previous figures are identified by the same reference symbols in Figs. 5 to 12, and will not be explained again.

Fig. 5 shows a schematic cross section through an interposer 5. This interposer 5 is produced from a printed circuit board 23 which is metallized on both sides and is structured on both sides. The metal structure on the upper face 36 of the printed circuit board 23 is connected to the metal structure on the lower face 40 of the printed circuit board 23 via through-contacts 26. The lower face 40 of the printed circuit board 23 has external contact surfaces 27, which are arranged in three rings on the lower face 40 of the printed circuit board 23. Interposer lines 21 are arranged on the upper face 36 of the printed circuit board 23, and are electrically connected to the through-contacts 26. In addition, the interposer lines 21

connect the through-contacts 26, and hence the external contact surfaces 27, to connecting pads 6 for flipchip connections 8 in a central area 7 of the printed circuit board 23, and/or to connecting pads 60 for the bonding connections 18 in edge areas 10 of the printed circuit board 23.

Fig. 6 shows a schematic cross section through an interposer 5 with a first electronics module 9 fitted to it. This electronics module 9 is connected via flipchip connections 8 to the connecting pads 6 in the central area 7 of the interposer 5. The intermediate space between the active upper face 35 of the first lower electronics module 9 and the upper face 36 of the interposer 5 is filled with an underfilling material 37.

Fig. 7 shows a schematic cross section through an electronics module 12 with an unprotected bonding channel 19. In addition to a semiconductor chip 3, which in this case is a memory chip 39, this second electronics module 12 has an interposer structure 13 with an intermediate substrate 41. Furthermore, the second electronics module 12 has a bonding channel 19 with central bonding connections 111, which are connected via the interposer structure 13 to external contact surfaces 14 on the electronics module 12.

An electronics module 12 which has been prepared in this way is subjected to extreme temperatures between -50 and 150°C before being installed in an electronic component, during which its serviceability is tested. This functional test is also carried out without the central bonding connections 111 in the bonding channel 19 having been protected in advance by a protective sheath.

Fig. 8 shows a schematic cross section through the second electronics module 12 as shown in Fig. 7 for a protected bonding channel 19. Owing to the protected bonding channel 19, the handling of the second electronics module 12 is easier and safer than the handling of an electronics module 12 with an unprotected bonding channel 19, as is shown in Fig. 7. This is because the sensitive central bonding connections 111 are embedded in a protective sheath 22, and are protected against mechanical damage during handling.

Fig. 9 shows a schematic cross section through a stack 4 comprising a first electronics module 9 and a second electronics module 12 on the interposer 5 as shown in Fig. 5. For this purpose, the second electronics module 12, which has been completely functionally tested, as shown in Fig. 7 or in Fig. 8, is adhesively bonded by its passive rear face 16 to the passive rear face 15 of the electronics module 9, by means of an adhesive layer 31.

Fig. 10 shows a schematic cross section through a stack 4 as shown in Fig. 9 after the fitting of bonding connections 11. These bonding connections 11 are fitted to the external contact surfaces 14 of the interposer structure 13 of the upper electronics module 12. For this purpose, a bonding head 33 is first of all bonded onto the external contact surfaces 14, and the bonding wire 18 is routed downwards to the connecting pads 60 on the interposer 5. The bonding wires 18 are then connected to the connecting pads 60, forming a bonding clip 34.

Fig. 11 shows a schematic cross section through an electronic component 1 after the stack 4 as shown in Fig. 10 has been packed in a component package 29. In this case, the lower face

40 of the interposer 5 at the same time forms the lower face of the electronic component 1. In addition, a material boundary 38 is formed between the material of the protective sheath 22 for the bonding channel 19 and the plastic packaging compound 17.

Fig. 12 shows a schematic cross section through an electronic component 1 after external contacts 30 have been fitted to the interposer 5. These external contacts 30 are in this case in the form of contact balls, and are arranged in three rings. This is done by soldering contact balls, which can be soldered, to the external contact surfaces 27 on the lower face 40 of the interposer structure 5.

Patent Claims

1. A method for producing an electronic component (1) with semiconductor chips (2, 3) in a stack (4), with the method having the following method steps:
a) provision of an interposer (5) with connecting pads (6) in a central area (7) for flipchip connections (8) for a lower electronics module (9), and with connecting pads (60) in edge areas (10) of the interposer (5) for bonding connections (11) for an upper electronics module (12),
b) fitting of the first lower electronics module (9), which is in the form of a semiconductor chip (2), using flipchip technology in the central area (7) of the interposer (5),
c) production of at least one second upper electronics module (12), which has a semiconductor chip (3) and an interposer structure (13) with external contact surfaces (14),
d) fitting of the upper electronics module (12) on the lower electronics module (9) such that the passive rear faces (15, 16) of the lower electronics module (9) and of the upper electronics module (12) are located one on top of the other,
e) production of bonding connections (11) between the external contact surfaces (14) of the upper electronics module (12) and the connecting pads (60) in the edge areas (10) of the interposer (5),
g) packing of the electronics modules (9, 12), with a plastic packaging compound (17) being fitted to the interposer (5).

2. The method as claimed in Claim 1,
characterized in that
the upper electronics module (12) is subjected to tests in extreme temperature conditions, in particular from -50°C to 150°C, before it is fitted to the passive rear face (15) of

the semiconductor chip (2) of the lower electronics module (9).

3. The method as claimed in Claim 1 or Claim 2, characterized in that at least one logic chip (28) is used as the first lower electronics module (9), and at least one memory chip (39) with external contact surfaces (14) is used as the second upper electronics module (12).

4. The method as claimed in one of Claims 1 to 3, characterized in that the upper electronics module (12) is adhesively bonded to the passive rear face (15) of the lower electronics module (9).

5. The method as claimed in one of Claims 1 to 4, characterized in that the bonding connections (11) between the external contacts (14) of the upper electronics module (12) and the connecting pads (60) on the interposer (5) are produced by means of wire bonds.

6. The method as claimed in one of Claims 1 to 5, characterized in that, in order to connect the connecting pads (60) in the edge areas (10) of the interposer (5) to the external contact surfaces (14) on the upper electronics module (12), bonding wires (18) are first of all bonded to the connecting pads (60), and are then bonded to the external contact surfaces (14).

7. The method as claimed in one of Claims 1 to 6,

characterized in that

a central bonding channel (19) is incorporated in the interposer structure (13) of the upper electronics module (12), and its bonding connections (111) are electrically conductively connected via bonding fingers (20) and via interposer lines (21) to the external contact surfaces (14).

8. The method as claimed in Claim 7,
characterized in that

the bonding channel (19) is covered by a protective sheath (22) of plastic with the bonding connections (111) being embedded.

9. The method as claimed in one of Claims 1 to 8,
characterized in that,

in order to produce an interposer (5), a first metal plating on a printed circuit board (23) which is metallized on both sides is structured with connecting pads (6) for flipchip connections in a central area (7), with connecting pads (60) for bonding connections (11) in edge areas (10) and with interposer lines (25) to through-contacts (26), with the through-contacts (26) being electrically connected to external contact surfaces (27) on a structured second metal plating on the printed circuit board (23).

10. The method as claimed in one of Claims 1 to 9,
characterized in that,

in order to pack the electronics modules, a filled epoxy resin is fitted by means of transfer molding methods to the interposer.

11. The method as claimed in one of Claims 1 to 9,
characterized in that,

in order to pack the electronics modules (9, 12), a plastic packaging compound is fitted by means of dispensing methods to the interposer (5).

12. The method as claimed in one of Claims 6 to 11, characterized in that external contacts (30) are fitted to the external contact surfaces (27) of the interposer (5).

13. An electronic component with semiconductor chips in a stack, with the electronic component (1) having the following features:

- an interposer (5) with connecting pads (6) for flipchip connections (8) in a central area (7), and with connecting pads (60) for bonding connections (11) in edge areas (10) of the interposer (5),
- at least one first lower electronics module (9) which is in the form of a semiconductor chip (2) and has contact areas (24) which are electrically connected using flipchip technology to the connecting pads (6) in the central area (7) of the interposer (5),
- at least one second upper electronics module (12), which has a semiconductor chip (3) and an interposer structure (13) with external contact surfaces (14) on the semiconductor chip (3), with the upper electronics module (12) being arranged on the lower electronics module (9) such that the passive rear faces (15, 16) of the electronics modules (9, 12) rest one on top of the other,
- bonding connections (11) between the external contact surfaces (14) of the upper electronics module (12) and the connecting pads (60) in the edge areas (10) of the interposer (5),

- a component package (29) which surrounds the electronics modules (9, 12).

14. The electronic component as claimed in Claim 13,
characterized in that
the protective sheath (22) has a material boundary (38) to the material of the component package (29).

15. The electronic component as claimed in Claim 13 or Claim 14,
characterized in that
the lower electronics module (9) is in the form of a logic chip (28), and in that the upper electronics module (12) is in the form of a memory chip (39) with an interposer structure (13) and with external contact surfaces (14).

16. The electronic component as claimed in one of Claims 13 to 15,
characterized in that
the interposer (5) has a printed circuit board (23) which is metallized and structured on both sides and has through-contacts (26) as an electrical connection between the structured metal layers on the upper face and on the lower face of the printed circuit board (23), with the lower face of the printed circuit board having external contact surfaces (27) with external contacts (30), and with the upper face of the printed circuit board having the connecting pads (6) for flipchip connections (8) in a central area (7), having the connecting pads (60) for bonding connections (11) in edge areas (10), and having interposer lines (25) between the connecting pads (6, 60) and the through-contacts (26).

17. The electronic component as claimed in one of Claims 13 to 16,

characterized in that

an adhesive layer (31) is arranged between the passive rear faces (15, 16) of the electronics modules (9, 12).

18. The electronic component as claimed in one of Claims 13 to 17,

characterized in that

the upper electronics module (12) has an active upper face (16) with a central bonding channel (19) with bonding connections (111), with the bonding connections (111) being connected to the external contact surfaces (14) via the interposer structure (13) which is arranged on the active upper face (32).

19. The electronic component as claimed in Claim 18,

characterized in that

the bonding channel (19), together with its bonding connections (111), has a protective sheath (22).

20. The electronic component as claimed in one of Claims 13 to 19,

characterized in that

the normal to the surface of the connecting pads (60) of the interposer (5) and the normals to the surface of the external contact surfaces (14) of the interposer structure (13) point in the same direction.

21. The electronic component as claimed in one of Claims 13 to 20,

characterized in that

the bonding connections (11) have a bonding wire (18) which forms a bonding clip (34), which runs from one of the connecting pads (60) on the interposer (5) to the corresponding external contact surface (14) on the upper electronics module (12).

Abstract

Electronic component with semiconductor chips in a stack, and a method for producing it

The invention relates both to a method for producing an electronic component (1), to semiconductor chips (2, 3) in a stack (4) and to an electronic component (1) such as this. The stack (4) has at least one first lower electronics module (9), which is connected via flipchip connections (8) to a central area (7) of an interposer (5). The stack (4) also has at least one second upper electronics module (12) with external contact surfaces (14), which are connected via bonding connections (11) to outer areas (10) of the interposer (5).

(Fig. 1)

List of reference symbols

1 Electronic component
2 Lower semiconductor chip
3 Upper semiconductor chip
4 Stack
5 Interposer
6 Connecting pads for flipchip connections
7 Central area of the interposer
8 Flipchip connections
9 Lower electronics module
10 Edge area of the interposer
11 Bonding connection
12 Upper electronics module
13 Interposer structure of the upper electronics module
14 External contact surfaces of the upper electronics module
15 Passive rear face of the lower electronics module
16 Passive rear face of the upper electronics module
17 Plastic packaging compound
18 Bonding wires
19 Bonding channel
20 Bonding finger
21 Interposer lines for the interposer structure
22 Protective sheath
23 Printed circuit board metallized on both sides
24 Contact areas
25 Interposer lines for the interposer
26 Through-contacts
27 External contact surfaces on the interposer
28 Logic chip
29 Component package
30 External contacts
31 Adhesive bonding layer
32 Active upper face of the upper electronics module
33 Bonding head
34 Bonding clip
35 Active upper face of the lower electronics module
36 Upper face of the interposer
37 Underfilling material
38 Material boundary
39 Memory chip
40 Lower face of the interposer
41 Intermediate substrate

60 Connecting pads for bonding connections
111 Central bonding connections